

OM SENI

ESD9L3.3ST5G, ESD9L5.0ST5G

Transient Voltage Suppressors

ESD Protection Diodes with Ultra-Low Capacitance

The ESD9L Series is designed to protect voltage sensitive components that require ultra-low capacitance from ESD and transient voltage events. Excellent clamping capability, low capacitance, low leakage, and fast response time, make these parts ideal for ESD protection on designs where board space is at a premium. Because of its low capacitance, it is suited for use in high frequency designs such as USB 2.0 high speed and antenna line applications.

Specification Features:

- Ultra Low Capacitance 0.5 pF
- Low Clamping Voltage
- Small Body Outline Dimensions:
0.039" x 0.024" (1.00 mm x 0.60 mm)
- Low Body Height: 0.016" (0.4 mm)
- Stand-off Voltage: 3.3 V, 5 V
- Low Leakage
- Response Time is Typically < 1.0 ns
- IEC61000-4-2 Level 4 ESD Protection
- These Devices are Pb-Free and are RoHS Compliant

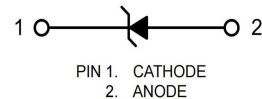
Mechanical Characteristics:

LEAD FINISH: 100% Matte Sn (Tin)

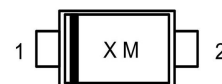
MOUNTING POSITION: Any

QUALIFIED MAX REFLOW TEMPERATURE: 260°C

Device Meets MSL 1 Requirements



MARKING DIAGRAM



X = Specific Device Code
M = Date Code

*Date Code orientation and/or position may vary depending upon manufacturing location.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
IEC 61000-4-2 (ESD) Contact Air		±10 ±15	kV
Total Power Dissipation on FR-5 Board (Note 1) @ T _A = 25°C	P _D	150	mW
Storage Temperature Range	T _{stg}	-55 to +150	°C
Junction Temperature Range	T _J	-55 to +150	°C
Lead Solder Temperature - Maximum (10 Second Duration)	T _L	260	°C

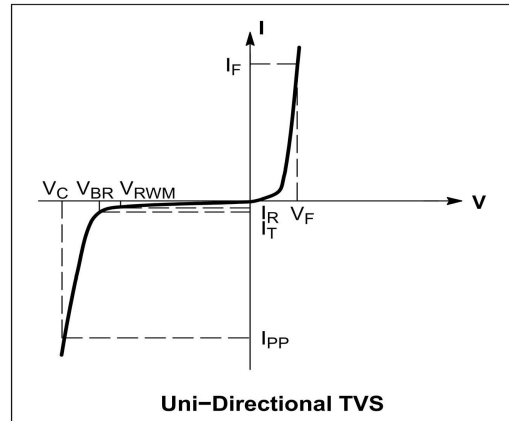
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ELECTRICAL CHARACTERISTICS

($T_A = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter
I_{PP}	Maximum Reverse Peak Pulse Current
V_C	Clamping Voltage @ I_{PP}
V_{RWM}	Working Peak Reverse Voltage
I_R	Maximum Reverse Leakage Current @ V_{RWM}
V_{BR}	Breakdown Voltage @ I_T
I_T	Test Current
I_F	Forward Current
V_F	Forward Voltage @ I_F
P_{pk}	Peak Power Dissipation
C	Max. Capacitance @ $V_R = 0$ and $f = 1.0$ MHz

*See Application Note AND8308/D for detailed explanations of datasheet parameters.



ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted, $V_F = 1.0$ V Max. @ $I_F = 10$ mA for all types)

Device*	Device Marking	V_{RWM} (V)	I_R (μA) @ V_{RWM}	V_{BR} (V) @ I_T (Note 2)	I_T	C (pF)		V_C (V) @ $I_{PP} = 1$ A	V_C
		Max	Max	Min	mA	Typ	Max	Max	Per IEC61000-4-2 (Note 4)
ESD9L3.3ST5G	6**	3.3	1.0	4.8	1.0	0.5	0.9	9.0	Figures 1 and 2 See Below
ESD9L5.0ST5G	D	5.0	1.0	5.4	1.0	0.5	0.9	9.8	Figures 1 and 2 See Below

*Includes S and SZ-prefix devices where applicable.

**Rotated 180° .

2. V_{BR} is measured with a pulse test current I_T at an ambient temperature of 25°C .

3. Surge current waveform per Figure 5.

4. For test procedure see Figures 3 and 4 and Application Note AND8307/D.

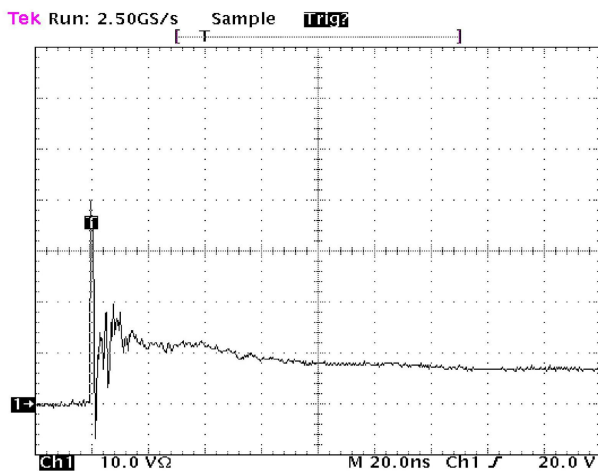


Figure 1. ESD Clamping Voltage Screenshot Positive 8 kV Contact per IEC61000-4-2

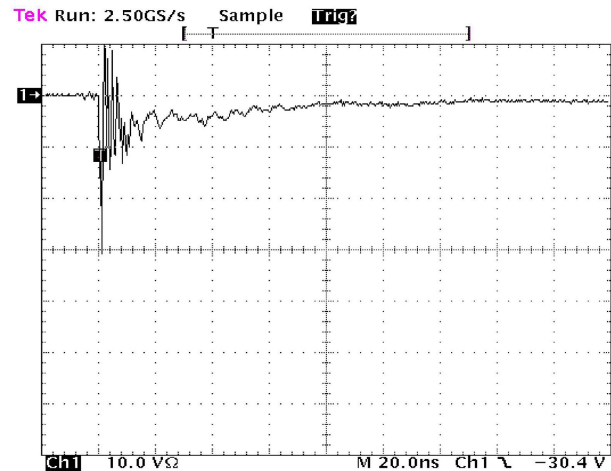


Figure 2. ESD Clamping Voltage Screenshot Negative 8 kV Contact per IEC61000-4-2

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IEC 61000-4-2 Spec.

Level	Test Voltage (kV)	First Peak Current (A)	Current at 30 ns (A)	Current at 60 ns (A)
1	2	7.5	4	2
2	4	15	8	4
3	6	22.5	12	6
4	8	30	16	8

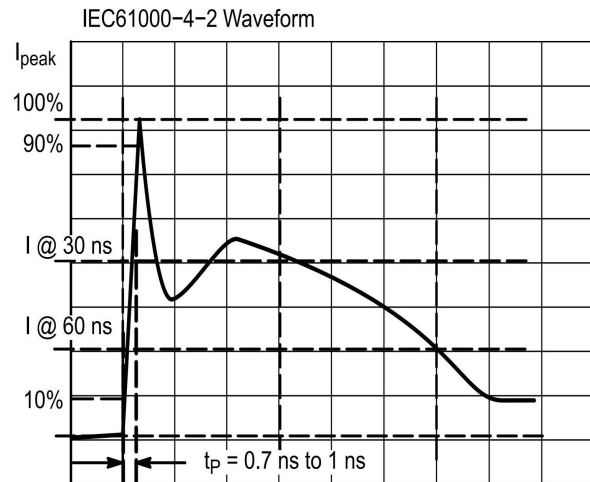


Figure 3. IEC61000-4-2 Spec

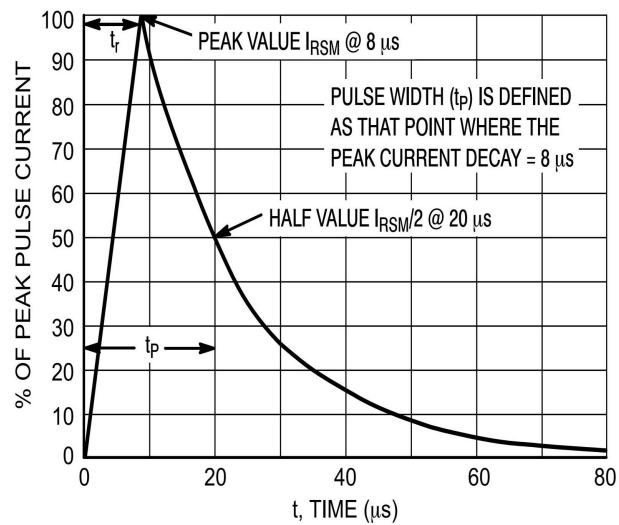


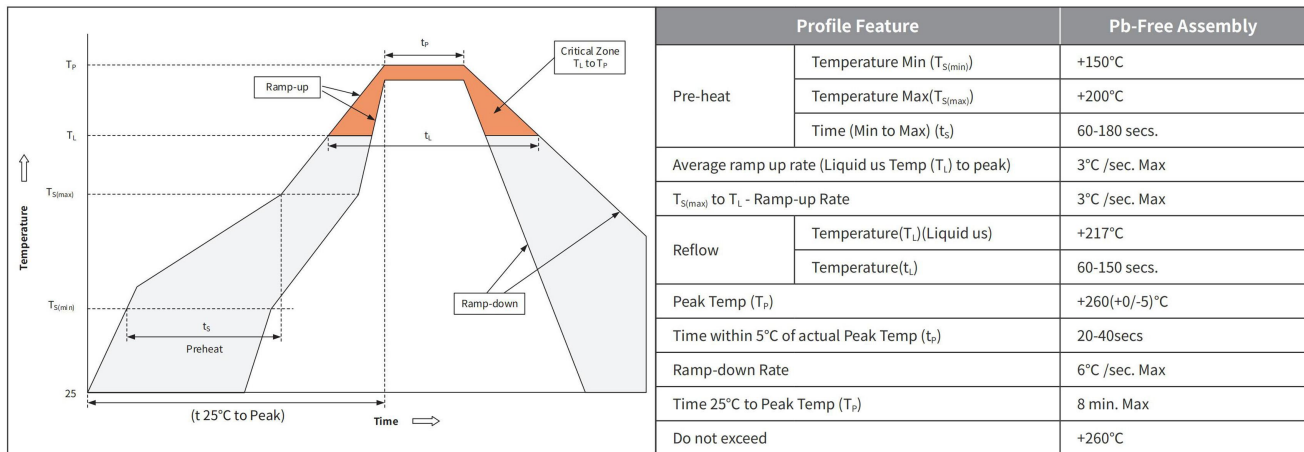
Figure 5. 8 X 20 μs Pulse Waveform

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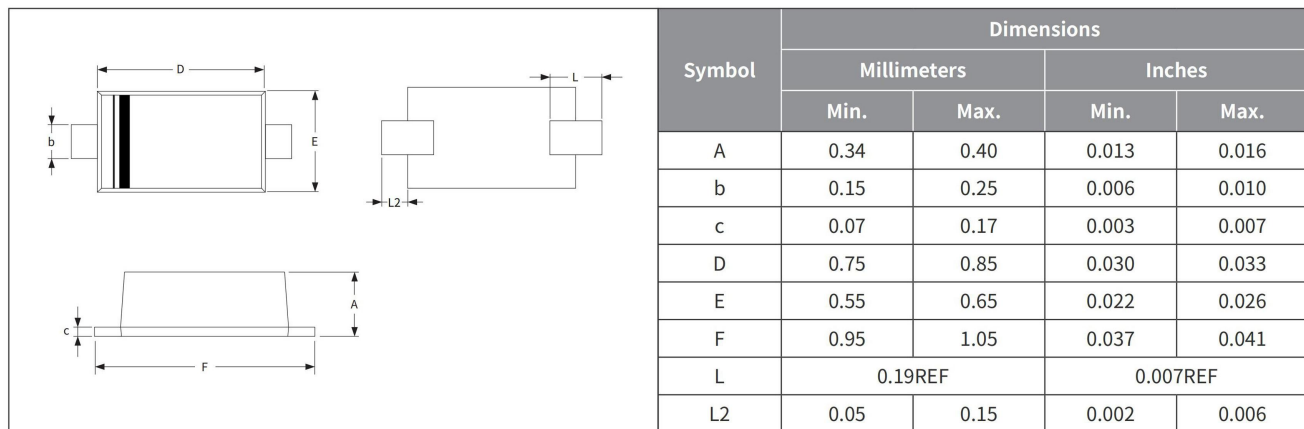
Ordering Information

PREFERRED P/N	PACKAGE	SIZE(mm)	DELIVERY MODE	MPQ(PCS)
	SOD-923	1.00×0.60×0.37	7"	8000

Recommended Soldering Conditions



Package Outline Dimensions (SOD-923)



Suggested Pad Layout

